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Comparative Study of Low Power Low Area Bypass Multipliers for Signal Processing Applications

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ABSTRACT
This paper presents a comparative study of 1-dimensional bypassing multipliers on basis of delay, area and power. If we can reduce the power consumption of the multiplier block, then we can reduce the power consumption of various digital signal processing chips and communication systems. In 2-dimensional bypass multiplier is presented the effective analysis of Slices, Lut, Cost & area is achieved. The implementation of Braun multipliers and its bypassing techniques is done using Verilog HDL using Xilinx 12.4 ISE. Results are showed and it is verified using the Spartan-3E and Synopsys respectively.
Keywords: Bypassing, Multipliers, Delay, Power, Area, Comparison.

I. INTRODUCTION

A multiplier is essential and abundant in DSP applications. Typical DSP applications where a multiplier plays an important role include image processing, wavelet transforms; telecommunication etc. The basic idea is to eliminate unnecessary computation of power saving via signal bypassing.

In newer technologies, power is a primary design constraint. The total power in the circuit is given by the following equation [1 2 6]

Total power = Switching power + Short circuit power+ Static power + leakage power

Where switching power caused by charging and discharging of node capacitance. Short-circuits is caused by simultaneous conduction of p and n blocks, Static dissipation due to leakage current. Dynamic power dissipation due to charging and discharging of load capacitances. The average dynamic dissipation of a CMOS gate is given by [1 2]

$$Pavg = 0.5* \alpha* C_L*Vdd^2*F_c$$

Where VDD is the supply voltage, α is the number of switching activity in a clock cycle.CL is the physical capacitance and fc is the clock frequency, In this paper comparison of various multiplier in means of power, cost & area and mixed bypass multiplier is analyzed with row and column bypass technique is presented.

The paper is organized as follows: In section 2 the comparison of multipliers are discussed.. In section 3 and 4 the experimental results and conclusion are discussed.

II. RELATED WORKS

2.1 PARALLEL ARRAY MULTIPLIER

Consider the multiplication of two unsigned n-bit numbers, where A = an–1 an–2 …a0 is the multiplicand and B = bn–1bn–2 …b0 is the multiplier. The product P = p2n–1, p2n–2 …p0.[3]

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                                  A3 A2 A1 A0

                                  B3 B2 B1 B0
                              ----------------------------
                                 A3.B0 A2.B0 A1.B0 A0.B0
                            A3.B1 A2.B1  A1.B1 A0.B1
                       A3.B2  A2.B2  A1.B2  A0.B2
                  A3.B3 A2.B3   A1.B3  A0.B3
-----------------------------------------------------------------
   P6       P5       P4     P3       P2     P1       P0
-----------------------------------------------------------------
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A 4X4 unsigned multiplication example is shown above[5 8 9]. The multiplicand Ai is added to the incoming partial product bit based on the value of the multiplier bit Bj Each row adds the multiplicand to the incoming partial product, PPi to generate the outgoing partial product PP(i+1), if Yi =1. If Yi=0, PPi is passed vertically down unchanged. Over the years the computational complexities of algorithms used in Digital Signal Processors (DSPs) have gradually increased. This requires a parallel array multiplier to meet the performance demands and a typical implementation of such an array multiplier is Braun design.

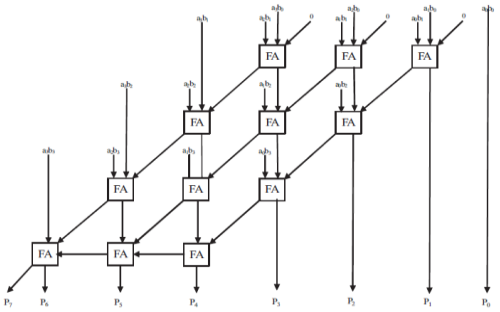


FIGURE- 1:-4x4 Braun multiplier

In the 4x4 Braun multiplier, the multiplier consists of 3 rows of carry-save adders, each rows have three full adder structures[3]. The full adder contains three inputs & two outputs: the sum bit and the carry a bit. Three FAs in the first CSA row that have only two valid inputs can be replaced by three half adders and three FAs in the last row can be constructed as a 3-bit ripple-carry adder.

2.2 LOW-POWER MULTIPLIER WITH ROW BYPASSING

The internal structure of the row-bypassing adder cell (RA) is shown below

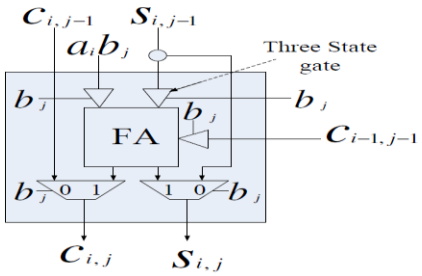


FIGURE.-2: Structure of FA (Row bypassing)

The design included (n-1)×(n-1) full adders, 2×(n-1)×(n-1) multiplexers, and 3×(n-1)×(n-1) three state gates.

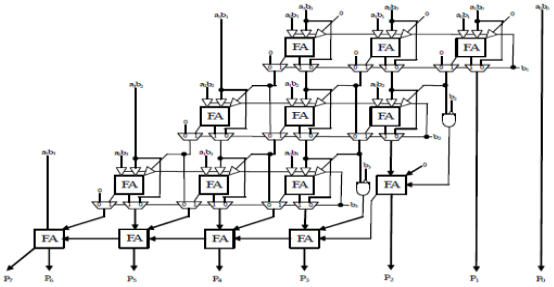


Figure-3: Row bypassing multiplier

When the corresponding partial product is zero, the FA & unnecessary transitions is disabled and bypassed the inputs to outputs. Two multiplexers augmented to the outputs of the adder transmit the input-carry bit and the input-sum bit of the previous addition to the outputs[4]. The tri-state buffers placed at the input of the adder cells disable signal transitions in the adders which are by passed, and then the input-carry bit and input-sum bit are passed to downwards. As shown in figure-2 & figure-3.Thus, the power consumption can be reduced if one can reduce the switching activity of a given logic circuit without changing its function. An obvious method to reduce the switching activity is to shut down the idle part of the circuit which is not in operating condition.

2.3 LOW-POWER MULTIPLIER WITH COLUMN BYPASSING

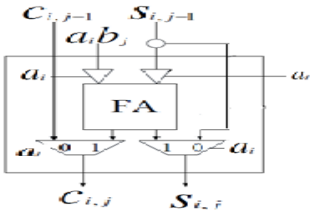


FIGURE-4: Structure of FA (column bypassing)

In the multiplier design, the modified FA is simpler than that in the row bypassing multiplier.[5 7] Each modified FA in the CSA array is only attached by two tri-state buffers and 2-to-1 multiplexer. As the bit ai in the multiplicand is 0, their inputs in the (i+1)-th column will be disabled and carry output in the column must be set to be 0 to produce correct output. Hence, the protecting process can be done by adding an AND gate at the outputs of the last. row of CSAs.

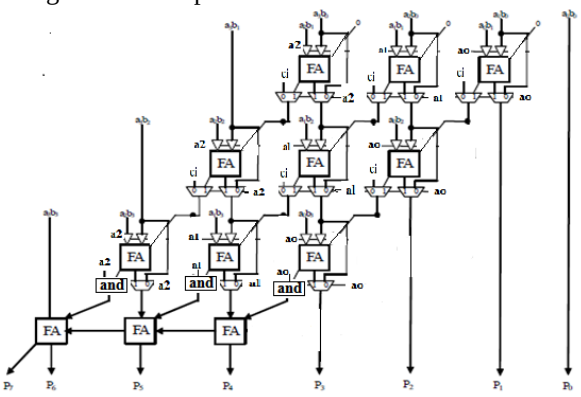


FIGURE-5: Column bypass multiplier

III. PROPOSED WORK

3.1 LOW POWER MULTIPLIER WITH MIXED BYPASSING

It is desired that in multiplier the addition operations in the i-th column or the j-th row can be

bypassed if the bit ai in the multiplicand is 0 or the bit bj in the multiplier is 0

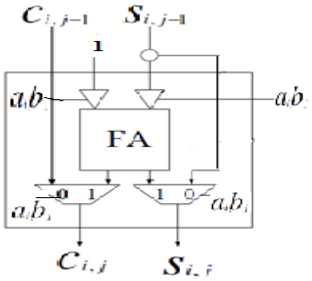


FIGURE -6: Structure of FA (Mixed bypassing)

The addition in the (i+1)-th column or j-th row can be by passed if the multiplicand bit, ai, or multiplier bit, bj, is 0.On the other hand, to get the correct carry propagation in a 2 dimensional bypassing scheme, the carry a bit from the previous row must be considered. Another multiplier design which is different to column-bypassing multiplier is mixed -bypassing multiplier. If the corresponding bit in the multiplicand and multiplier is 0, the operations in a column can be disabled. Consider the multiplier in Figure 6, the tri-state buffers placed at the input of the adder cells, if the buffer state is one, disable signal transitions in the adders which are bypassed, and then the input-sum bit are passed to downwards. When the corresponding partial product is zero, the CA disabled unnecessary transitions and bypassed the inputs to outputs. In other words, there are two bits to be added, and the output-carry bit must be zero, and the output-sum bit is equal to input-sum bit. The operations in column i can be ignored and the adders can be disabled since the output are known. The design included (n-1)×(n-1) full adders, (n-1)×(n-1) multiplexers, and 2×(n-1)×(n-1) three state gates.

IV. EXPERIMENTAL RESULTS

In order to evaluate the performance of low power parallel multiplier, all above designs are simulated in Spartan 3E FPGA device .The performance of this design with array multiplier, row bypassing, and column bypassing, mixed bypassing multipliers.

First, the Braun multiplier which removes the extra correction circuitry needed. But the limitation of this technique is that it cannot stop the switching activity even if the bit coefficient is zero so the power & area consumption is high. Next, in the row bypassing technique extra correction circuitry is needed and the structure of full adder is difficult.. It is one of the demerits of this technique In terms of power & area, the power consumed by this technique is less but area was high when compared to Braun multiplier.

In column bypassing technique the power consumed was low but the area was high comparatively to the Braun multiplier. In the case of mixed bypassing technique the power & area were low when compared with Braun multiplier

But in term of area the mixed bypass multiplier is low when compared to all other multiplier techniques, which further reduces the cost, Hence this paper conclude that the mixed bypass technique is very effective in CMOS circuitry in VLSI design.

The design was synthesized on Xilinx 12.1.The synthesized results on Xilinx XST are shown below in table 1 and 2 respectively.[10]

TABLE 1: Synthesis result on x Power Tool

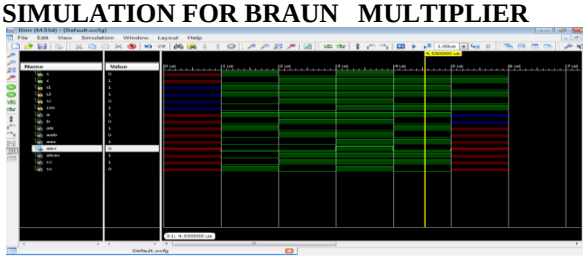
Multiplier type	**Array multiplier**	**Row bypass**	**Column bypass**	**Mixed bypass**
Vendor	xilinx	xilinx	xilinx	xilinx
Device and family	Spartan 3E	Spartan 3E	Spartan 3E	Spartan 3E
Logic power	0.00136	0.00020	0.00004	0.00092
Signal power	0.00053	0.00024	0.00015	0.00049
Total power(w)	0.00189	0.00044	0.00019	0.00141

TABLE 2: SYNTHESIS RESULT ON XILINIX XST

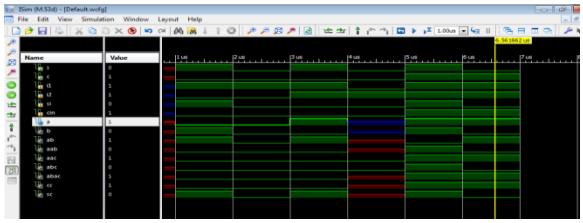
Multiplier type	Array multiplier	Row bypass	Column bypass	Mixed bypass
No. slices	19	27	33	19
LUT	35	48	61	33

SIMULATION RESULTS:

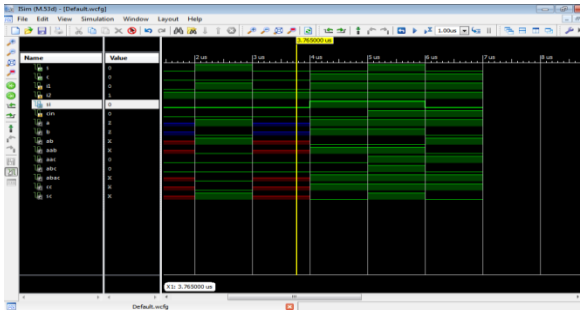
SIMULATION FOR BRAUN MULTIPLIER



SIMULATION FOR ROW BYPASS MULTIPLIER



SIMULATION FOR COLUMN BYPASS MULTIPLIER



SIMULATION FOR MIXED BYPASS MULTIPLIER

V. CONCLUSION

This paper concludes that, after comparing all the multiplier mixed bypass multiplier is best suited for situations where both area and cost are low. The number of slices & lut used is also less when compared to other techniques. Hence the mixed bypass multiplier is effective in dsp applications of VLSI design

VI. FUTURE WORK

The work can been done for 8*8 and 16*16 & 32 *32 etc unsigned multipliers. The bypassing techniques with the architectural modifications can also be applied to signed array multiplier architectures.

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